# Changes to Commands and Properties

## Command Changes

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| --- | --- |
| **Command Name** | **Comment** |
| set\_ivc\_ovc\_mapping | New command to set the mapping between an input VC at a router port and an output port on the same router. |
| reset\_ivc\_ovc\_mapping | New command to reset the mapping between an input VC at a router port and an output port |
| list\_ivc\_ovc\_mapping | New command to to list the input VC to output VC mapping on a router. |
| assert\_group\_clocks | New command to check that the specified rtl group has no clocks other than the listed clocks |
| list\_curves | New command to list the points of a curve/probability mass function or show all curves/probability mass functions |
| set\_curve | New command to set the piecewise linear curve associated with a name. |
| reset\_map | New command to reset the mapping of traffic. |
| enter\_tcl\_mode | New command to enable use of the TCL interpreter to process further input |
| exit\_tcl\_mode | New command to return to processing NCF input format from TCL mode |
| ml\_build | New command to build NoCs using machine learning |

## Default Property Changes

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| --- | --- | --- |
| **Property Name** | **Default Value** | **Comment** |
| read\_burstiness | 1 | This property has been replaced by new property burstiness |
| burstiness | 1 | This property is meant to replace read\_burstiness |
| noc\_injection\_queue\_depth | 0 | This property has been replaced by niq\_depth |
| niq\_depth | 0 | This property is meant to replace noc\_injection\_queue\_depth |
| noc\_ejection\_queue\_depth | 0 | This property has been replaced by neq\_depth |
| neq\_depth | 0 | This property is meant to replace noc\_ejection\_queue\_depth |
| host\_processing\_queue\_depth | 32 | This property has been renamed to hpq\_depth |
| hpq\_depth | 32 | This property has replaced host\_processing\_queue\_depth |
| trace\_enable | no | This property has been deprecated |
| axi4\_ac\_parity\_enb | no | New property to enable parity on all AC channels |
| axi4\_acaddr\_parity\_enb | no | New property to enable parity for addresses on all AC channels |
| axi4\_ar\_parity\_enb | no | New property to enable parity on all AR channels |
| axi4\_araddr\_parity\_enb | no | New property to enable parity for addresses on all AR channels |
| axi4\_aw\_parity\_enb | no | New property to enable parity on all AW channels |
| axi4\_awaddr\_parity\_enb | no | New property to enable parity for addresses on all AW channels |
| axi4\_bresp\_parity\_enb | no | New property to enable parity on all B response channels |
| axi4\_cd\_parity\_enb | no | New property to enable parity for data on all CD channels |
| axi4\_w\_parity\_enb | no | New property to enable parity for data on all W channels |
| ppln\_in\_node\_id\_pd | no | New property to enable the use of node PDs for pipeline stages |
| guaranteed\_sink | no | New property that forces the interface to sink every packet that it receives without any backpressue into the NoC |
| prefer\_shortest\_path\_routes | yes | New property to prefer shortest path routes with more turns over longer routes with fewer turns in route computation between 2 points |
| synchronizer\_depth | 2 | This property is used to set the default depth of clock synchronizers inserted by NocStudio |
| axi4s\_drain\_b\_response | yes | New property that indicates whether axi4s devices have preallocated space for B response packets to drain into the bridge |
| axi4s\_r\_interleave | no | New property that indicates whether axi4s devices can send interleaved read data. |
| axi4\_allow\_different\_data\_widths | no | New property to allow read response and write request channels to have different data widths. |
| axi4m\_ar\_rob\_ram\_enable | no | New propety to enable use of RAMs instead of flops for the read reorder buffer |
| cc\_pfb\_ram\_enable | no | New propety to enable use of RAMs instead of flops for the CCC prefetch buffer |
| cc\_pfb\_ram\_in\_width | 0 | New property to set the number of bits of input for CCC prefetch buffer RAMs. |
| cc\_pfb\_ram\_out\_width | 0 | New property to set the number of bits of output for CCC prefetch buffer RAMs. |
| axi4m\_ar\_rob\_ram\_in\_width | 0 | New property to set the number of bits of input for read reorder buffer RAMs. |
| axi4m\_ar\_rob\_ram\_out\_width | 0 | New property to set the number of bits of output for read reorder buffer RAMs. |
| iocb\_master\_port\_rd\_buffer\_ram\_enable | no | New propety to enable use of RAMs instead of flops for the IOCB master port read buffer |
| iocb\_master\_port\_rd\_buffer\_ram\_in\_width | 0 | New property to set the number of bits of input for the IOCB master port read buffer RAMs. |

## Mesh Property Changes

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| --- | --- | --- |
| **Property Name** | **Default Value** | **Comment** |
| enable\_direct\_host\_connection | yes | New property to allow the deletion of bridges on 2 different hosts such that their hosts are directly wired together. |
| intf\_parity\_addr\_per\_byte | yes | New property to choose between per byte or per word parity for addresses in the NoC |
| intf\_parity\_per\_byte | no | New property to choose between per byte or per word parity in the NoC |

## Bridge Property Changes

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| --- | --- |
| **Property Name** | **Comment** |
| trace\_enable | New property to enable tracing on ACE bridges |
| axi4m\_ar\_rob\_ram\_enable | New propety to enable use of RAMs instead of flops for the read reorder buffer |
| axi4m\_ar\_rob\_ram\_in\_width | New property to set the number of bits of input for read reorder buffer RAMs. |
| axi4m\_ar\_rob\_ram\_out\_width | New property to set the number of bits of output for read reorder buffer RAMs. |
| axi4s\_drain\_b\_response | New property that indicates whether axi4s devices have preallocated space for B response packets to drain into the bridge |
| axi4\_allow\_different\_data\_widths | New property to allow read response and write request channels to have different data widths. |
| acels\_support\_cache\_maintenance | New property to allow ACELS bridges to receive cache maintenance operations |
| axi4\_ac\_parity\_enb | New property to enable parity on the AC channel |
| axi4\_acaddr\_parity\_enb | New property to enable parity for addresses on the AC channel |
| axi4\_ar\_parity\_enb | New property to enable parity on the AR channel |
| axi4\_araddr\_parity\_enb | New property to enable parity for addresses on the AR channel |
| axi4\_aw\_parity\_enb | New property to enable parity on the AW channel |
| axi4\_awaddr\_parity\_enb | New property to enable parity for addresses on the AW channel |
| axi4\_bresp\_parity\_enb | New property to enable parity on the B response channel |
| axi4\_cd\_parity\_enb | New property to enable parity for data on the CD channel |
| axi4\_r\_parity\_enb | New property to enable parity for data on the R channel |
| axi4\_w\_parity\_enb | New property to enable parity for data on the W channel |
| axi4\_rresp\_parity\_enb | New property to enable parity on the R response channel |

## Host Property Changes

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| --- | --- |
| **Property Name** | **Comment** |
| llc\_class0\_alloc\_waygroups | This property has been replaced by llc\_class0\_alloc\_ways |
| llc\_class1\_alloc\_waygroups | This property has been replaced by llc\_class1\_alloc\_ways |
| llc\_class2\_alloc\_waygroups | This property has been replaced by llc\_class2\_alloc\_ways |
| llc\_class3\_alloc\_waygroups | This property has been replaced by llc\_class3\_alloc\_ways |
| llc\_class4\_alloc\_waygroups | This property has been replaced by llc\_class4\_alloc\_ways |
| llc\_class5\_alloc\_waygroups | This property has been replaced by llc\_class5\_alloc\_ways |
| llc\_class6\_alloc\_waygroups | This property has been replaced by llc\_class6\_alloc\_ways |
| llc\_class7\_alloc\_waygroups | This property has been replaced by llc\_class7\_alloc\_ways |
| llc\_class0\_alloc\_ways | This property is meant to replace llc\_class0\_alloc\_waygroups |
| llc\_class1\_alloc\_ways | This property is meant to replace llc\_class1\_alloc\_waygroups |
| llc\_class2\_alloc\_ways | This property is meant to replace llc\_class2\_alloc\_waygroups |
| llc\_class3\_alloc\_ways | This property is meant to replace llc\_class3\_alloc\_waygroups |
| llc\_class4\_alloc\_ways | This property is meant to replace llc\_class4\_alloc\_waygroups |
| llc\_class5\_alloc\_ways | This property is meant to replace llc\_class5\_alloc\_waygroups |
| llc\_class6\_alloc\_ways | This property is meant to replace llc\_class6\_alloc\_waygroups |
| llc\_class7\_alloc\_ways | This property is meant to replace llc\_class7\_alloc\_waygroups |
| llc\_waygroup\_cache\_mode\_enable | This property has been replaced by llc\_way\_cache\_mode\_enable |
| llc\_waygroup\_ram\_mode\_enable | This property has been replaced by llc\_way\_ram\_mode\_enable |
| llc\_waygroup\_ram\_mode\_secure | This property has been replaced by llc\_way\_ram\_mode\_secure |
| llc\_way\_cache\_mode\_enable | This property is meant to replace llc\_waygroup\_cache\_mode\_enable |
| llc\_way\_ram\_mode\_enable | This property is meant to replace llc\_waygroup\_ram\_mode\_enable |
| llc\_way\_ram\_mode\_secure | This property is meant to replace llc\_waygroup\_ram\_mode\_secure |
| cc\_data\_width | This property is used to change the data width of IOCB hosts |
| cc\_pfb\_ram\_enable | New propety to enable use of RAMs instead of flops for the CCC prefetch buffer |
| cc\_pfb\_ram\_in\_width | New property to set the number of bits of input for CCC prefetch buffer RAMs. |
| cc\_pfb\_ram\_out\_width | New property to set the number of bits of output for CCC prefetch buffer RAMs. |
| iocb\_master\_port\_rd\_buffer\_ram\_enable | New propety to enable use of RAMs instead of flops for the IOCB master port read buffer |
| iocb\_master\_port\_rd\_buffer\_ram\_in\_width | New property to set the number of bits of input for the IOCB master port read buffer RAMs. |
| iocb\_master\_port\_rd\_buffer\_ram\_out\_width | New property to set the number of bits of output for the IOCB master port read RAMs. |
| iocb\_slave\_port\_wr\_buffer\_ram\_enable | New propety to enable use of RAMs instead of flops for the IOCB slave port write buffer |
| iocb\_slave\_port\_wr\_buffer\_ram\_in\_width | New property to set the number of bits of input for the IOCB slave port write buffer RAMs. |
| iocb\_slave\_port\_wr\_buffer\_ram\_out\_width | New property to set the number of bits of output for the IOCB slave port write RAMs. |
| llc\_master\_port\_wr\_buffer\_ram\_enable | New propety to enable use of RAMs instead of flops for the LLC master port read buffer |
| llc\_master\_port\_wr\_buffer\_ram\_in\_width | New property to set the number of bits of input for the LLC master port read buffer RAMs. |
| llc\_master\_port\_wr\_buffer\_ram\_out\_width | New property to set the number of bits of output for the LLC master port read RAMs. |
| llc\_slave\_port2\_rd\_buffer\_ram\_enable | New propety to enable use of RAMs instead of flops for the LLC second slave port write buffer |
| llc\_slave\_port2\_rd\_buffer\_ram\_in\_width | New property to set the number of bits of input for the LLC second slave port write buffer RAMs. |
| llc\_slave\_port2\_rd\_buffer\_ram\_out\_width | New property to set the number of bits of output for the LLC second slave port write RAMs. |
| llc\_slave\_port\_rd\_buffer\_ram\_enable | New propety to enable use of RAMs instead of flops for the LLC slave port write buffer |
| llc\_slave\_port\_rd\_buffer\_ram\_in\_width | New property to set the number of bits of input for the LLC slave port write buffer RAMs. |
| llc\_slave\_port\_rd\_buffer\_ram\_out\_width | New property to set the number of bits of output for the LLC slave port write RAMs. |

## Interface Property Changes

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| --- | --- |
| **Property Name** | **Comment** |
| noc\_injection\_queue\_depth | This property has been replaced by niq\_depth |
| niq\_depth | This property is meant to replace noc\_injection\_queue\_depth |
| noc\_ejection\_queue\_depth | This property has been replaced by neq\_depth |
| neq\_depth | This property is meant to replace noc\_ejection\_queue\_depth |
| host\_processing\_queue\_depth | This property has been replaced by hpq\_depth |
| hpq\_depth | This property is meant to replace host\_processing\_queue\_depth |
| hpq\_latency\_curve | This property is used to automatically control host processing latency based on the specified curve |
| hpq\_latency | This property is used to automatically control host processing latency based on the specified constant value. |
| hpq\_rate\_curve | This property is used to automatically control host processing completion rate. |
| hpq\_rate | This property is used to automatically control host processing completion rate based on a specified constant value. |
| shared\_hpq | This property is used to control the host processing queue that requests arriving at this interface should go to. |
| guaranteed\_sink | This property forces the interface to sink every packet that it receives without any backpressue into the NoC |
| atid | This property specifies the ATB ID of the element |
| trace\_fifo\_depth | This property specifies the size of the trace capture buffer for this interface. |
| ext\_timestamp\_value | This property is used to enable use of TSVALUE interface to produce timestamps from time source external to bridge. |
| timestamp\_width | This property is used to specify the bit width of timestamp values captured in trace streams. |
| trace\_req\_capture\_mask | This property is used to specify the bit mask that controls which fields are captured for this interface. |
| trace\_resp\_capture\_mask | This property is used to specify the bit mask that controls which fields are captured for this interface. |
| atb\_fifo\_depth | This property is used to specify the size of the ATB data buffer for this interface |

## Link Property Changes

None

## Router Property Changes

None

## VC Property Changes

None